Lab Number 5 Report

Ben Simpson, Section # 001

Benjamin Bergeson, Section # 001

**Introduction**

In this lab, we will be building the receiver board for the laser tag system. This circuit amplifies the signal from the photodiode receiver so that it can be read by the Zybo Board. Using this signal, the board can then determine whether or not the player has been shot.

The basic design for the receiver board circuit involves three parts: the photodiode/resistance combination, the voltage amplification stage, and the voltage limiter. The photodiode/resistance stage converts the current generated by the photodiode into voltage using a 3.3 kΩ resistor as a voltage divider. This stage provides some of the amplification necessary to meet the requirement of a gain between 5 and 10 million V/A. The rest of the necessary gain comes from the voltage amplification stage, which uses BJTs to amplify the voltage. The final part of the circuit, the voltage limiter, ensures that the output voltage is less than 1 Vpp by clipping the signal for high currents produced by the photodiode, thus allowing the signal to be passed to the Zybo Board under a variety of input conditions.

In addition to amplifying the signal from the photodiode, the receiver filters out extraneous signals, since the guns use only a limited range of frequencies for identification when shooting. The receiver board is also designed to consume very little power since it runs off of a 9V battery. The full specifications of the receiver board are detailed below.

**Specifications**

These are the specifications for the receiver board:

* Gain: 5x106 V/A – 10x106 V/A
* Maximum output voltage: 1V
* Bandpass filter built into amplifier
  + At least second order with 10 kHz<fH<20 kHz
* Total current draw less than 1mA
* Output impedance less than 500W

**Voltage Amplifier Design**

Since the photodiode/resistor part of the receiver board circuit produces a gain of 3300 V/A, in order to obtain a total gain of between 5 and 10 million V/A, our voltage amplification stage would need to be between 1500 and 3000 V/V. We decided to use three stages of around 13 V/V gain each in order to create a total gain of about 2200 V/V in the amplification stage, which translates to a gain of 7.2x10­6 V/A in the overall receiver board. In order to achieve the necessary gain between in each of the stages, we decided that we needed a CE amplifier followed by a CC amplifier in each stage. The CE amplifier would produce most of the voltage gain while the CC amplifier would act as a buffer in order to reduce loading. This brought the total number of BJTs up to six.

Using the same formulas as lab 4 we were able to determine the values for the CE stage of the amplifier. Since the gain of a CE amplifier is approximately equal to Rc/Re, we chose that ratio to be 15. We determined that this would give us enough gain to still achieve our goal of 13 V/V even after losses due to loading between stages. We chose Rc = 150 kΩ and Re = 10 kΩ so that the power draw through the circuit would be low.

The values of R1 and R2 were selected to create a voltage divider so that the BJT is in the active regime. Since the supply voltage used in the circuit is 9 V, our original design was to center the output voltage of the CE amplifier at 4.5 V for maximum headroom in amplifying the signal. After attempting that biasing and having it not work, we realized that this was unrealistic since the 15:1 ratio between Rc and Re would push the voltage at the output node far below 4.5 V. Using LTSpice, we adjusted the values of R­1 and R2 until our desired gain was achieved.

The circuit and the resistor values for the CE stage can be seen in Figure 1.

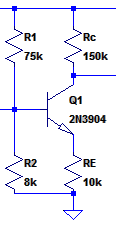


Figure 1 Initial values for the CE stage

For the CC stage, our main goal was to reduce loading between it and the CE stage. In order to do this, we made the input impedance of the CC stage much higher than the output impedance of the CE stage. The output impedance of the CE stage is Rc which we selected to be 150 kΩ, so we wanted the input impedance of the CC stage to be at least 10 times that, or 1.5 MΩ. The input impedance of our CC stage is given by the equation:

Rin = (Rπ + βRe + Rb) || R3 || R4 (Eq. 1)

R3 and R4 are the biasing resistors at the base of the BJT. We chose the values of R3 and R4 to be above 3 MΩ, which would give Rin a value of at least 1.5 MΩ provided that the summation term in the parallel resistor combination in (Eq. 1) could be ignored. We then assumed that β = 300 and chose Re of the CC stage to be 100 kΩ, making the sum at the left of (Eq. 1) a value of approximately 30 MΩ. Since this is much larger than R3 and R4, we could now ignore the term entirely in the computation as we had desired to do.

Once the CE and CC amplifiers were designed, we put them together into a single circuit and made some adjustments in LTSpice until it worked. This resulting circuit can be seen in Figure 2. Note that coupling capacitors are used between the two stages to maintain the correct bias points.

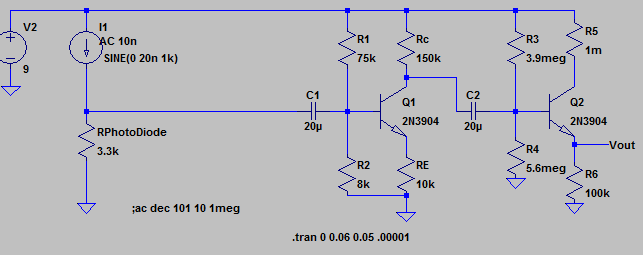


Figure 2 circuit for combination of CE and CC stages

We then duplicated the two amplifiers and added them together to create our envisioned six stage amplifier. With all six stages, the voltage amplifier should have had a total gain of around 2200 V/V, which was our goal.

**Bandpass Filtering**

Now that the voltage amplifier had the correct gain, we altered the design slightly so that it would act as a 2nd order bandpass filter as described in the specifications. We chose a lower corner frequency of 150 Hz and an upper corner frequency of 15 kHz. Using the schematic values we were able to calculate the capacitors needed to achieve our upper and lower corner frequencies.

For the lower corner frequency, we decided to adjust the value of the coupling capacitor between the 2nd CC stage and the 3rd CE stage. In order to calculate the value of the capacitor needed for the lower corner frequency, we first had to calculate the Rin of the CE BJT. The calculations for the Rin of the CE BJT and the lower corner frequency can be seen in Figures 3 and 4 respectively.

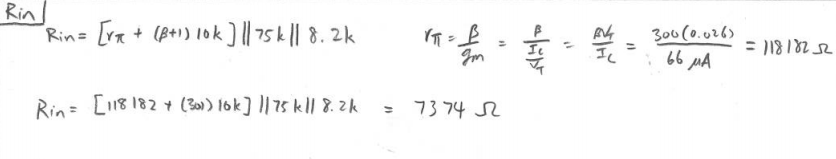


Figure 3. Calculations for Rin of the 3rd CE stage

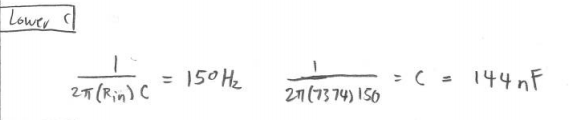


Figure 4 calculations for lower corner frequency capacitor

To create the upper corner frequency, we added a capacitor in from the node between the 3rd CE and CC stages to ground. The value of this capacitor can be determined by using the output impedance of the 3rd CE stage. The type of calculation that we used to determine the capacitor value needed to achieve our upper corner frequency can be seen in Figure 5.

(Note that the value for the output impedance of 3rd CE stage does not match its predicted value from Figure 2. This calculation was made after some circuit tuning had already taken place. To match the circuit in Figure 2, the value 120k—which is the output impedance, in ohms, of the 3rd CE stage—should be replaced with 150k. The corresponding capacitor value is 70.7 pF.)

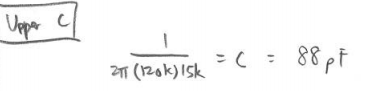


Figure 5 Sample calculation for upper corner frequency

**Voltage Limiter Design**

With the voltage amplification stage complete, we moved on to the voltage limiter. In order to limit the output voltage, we placed a diode in parallel with the output, so that the output could not get higher than the diode’s turn-on voltage. Figure 6 shows entire circuit up to this point.

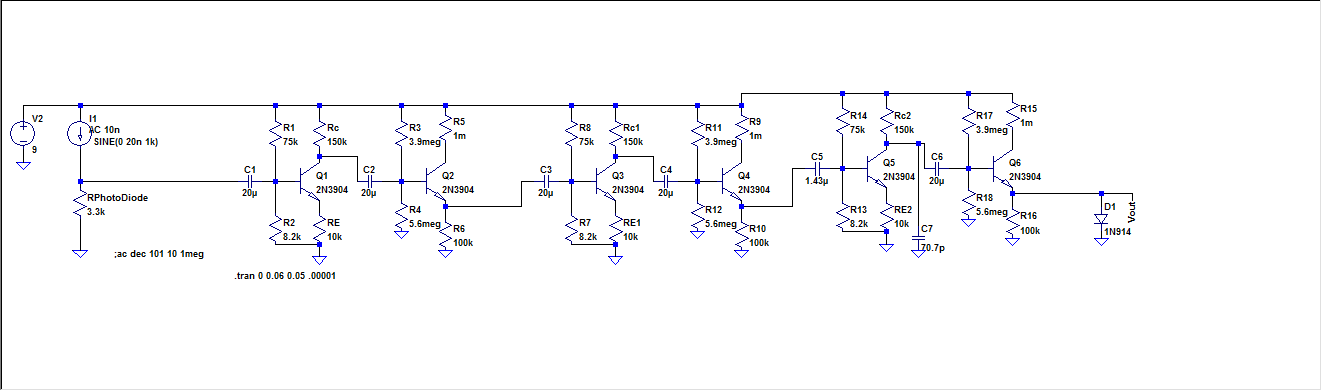


Figure 6 Full circuit diagram before tuning.

After adding the diode, we noticed that the gain had been cut drastically in our circuit simulations. We eventually determined that the diode had lowered the voltage on the emitter of the 3rd CC stage and put it into saturation. We simply adjusted the biasing on the base of that BJT, and our gain returned.

**Simulations**

After obtaining our basic design, we ran simulations and made further adjustments to the stages in order to meet the specs. The first simulation that we ran that met the gain specification can be seen in Figure 7. This yielded a gain of 5.71E6 V/A, which is within the specified 5E6 and 10E6 V/A.

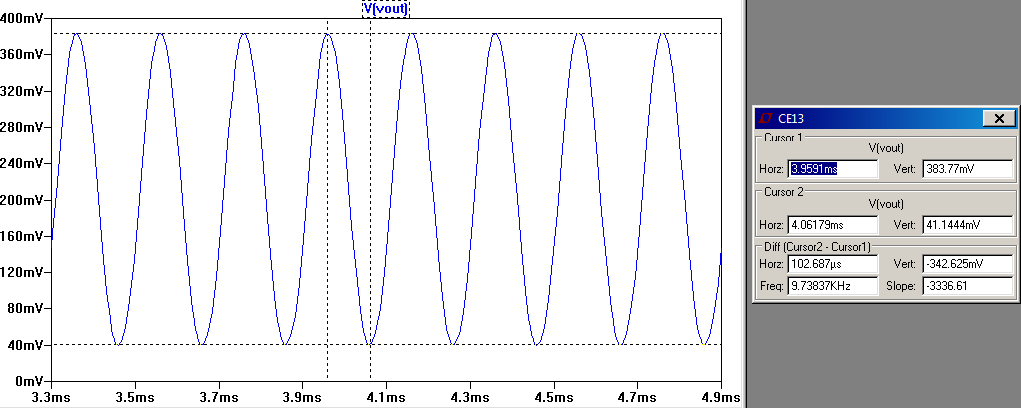


Figure 7 Gain simulation

We also ran frequency response simulations in order to determine that our voltage amplifier was performing its bandpass filtering correctly. We needed to slightly adjust our calculated capacitances in order for our corner frequencies to be where we want them to be. We ultimately adjusted the capacitance for the lower corner frequency to be 165nF and the capacitance for our upper corner frequency to be 140 pF. The simulation for the lower and upper corner frequency can be seen in Figure 8 and 9 respectively.

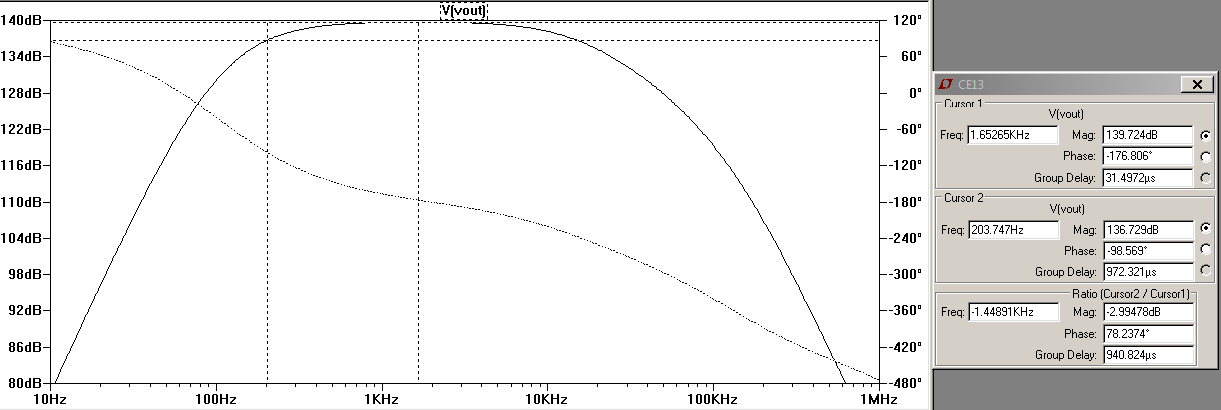


Figure 8 lower corner frequency

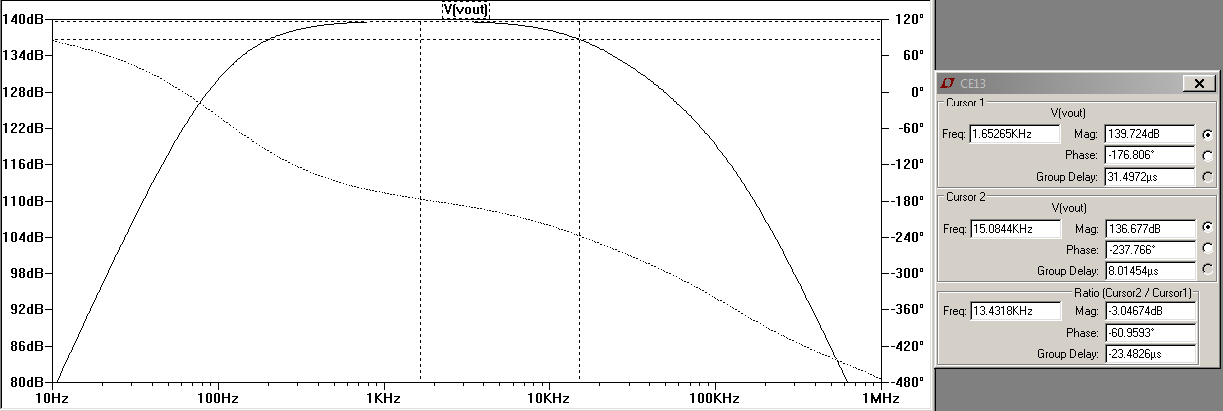


Figure 9 upper corner frequency

/\*\*\*\*\*\*\*\*\*\*\*\* DONE UNTIL HERE \*\*\*\*\*\*\*\*\*\*\*\*\*\*/

To do:

-Put in the voltage limiting simulation from down below.

-Note the differences between the final schematic and the one in Figure 6

-Rename figures

-Write conclusion

Now that we have a circuit that meets some of the specifications, we need to make sure that it meets the specification for output impedance. The calculations for the output impedance of the circuit can be seen in figure 15.

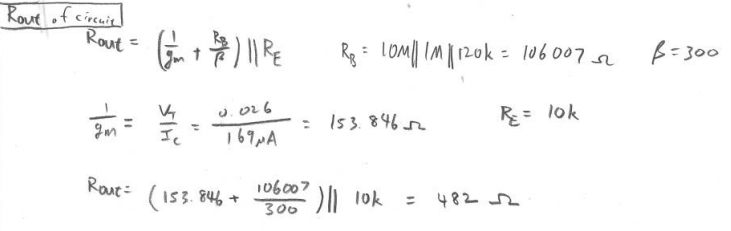


Figure 10 output impedance of the whole circuit

In order to test the power consumption of our circuit, we put a 20 nA input and then a 100 µA input to see if either one of them drew too much power from the power source. The simulations for both can be seen in figure 16 and 17 respectively.

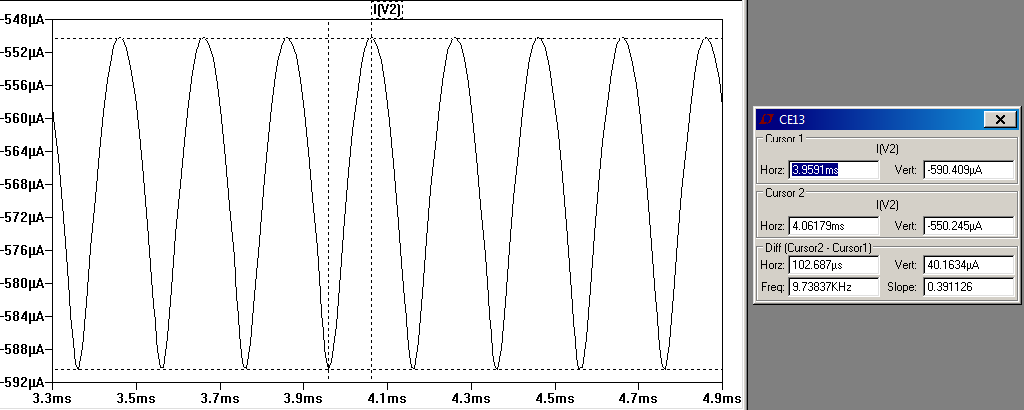


Figure 11 power consumption at 20 nA

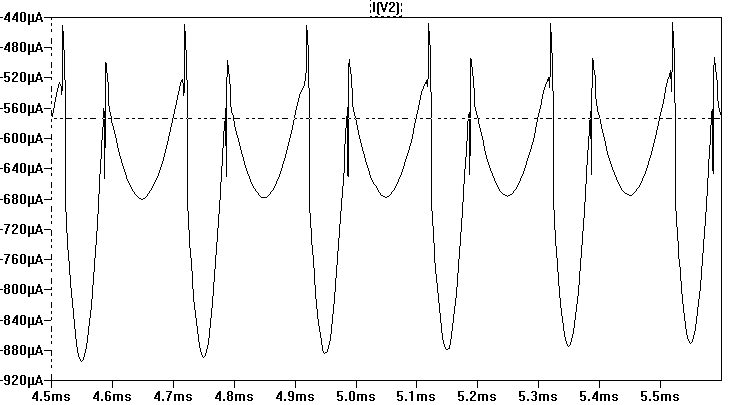


Figure 12 power consumption at 100 µA

Now that we have a complete schematic that works in theory, we started building our circuit on the breadboard. As we went along, we ran into problems and found ways to solve them. Most of them involved changing the circuit resistors. These changes will be mentioned later when we go into detail about building the circuit on the breadboard. After all the tuning we have our final schematic (figure 18).

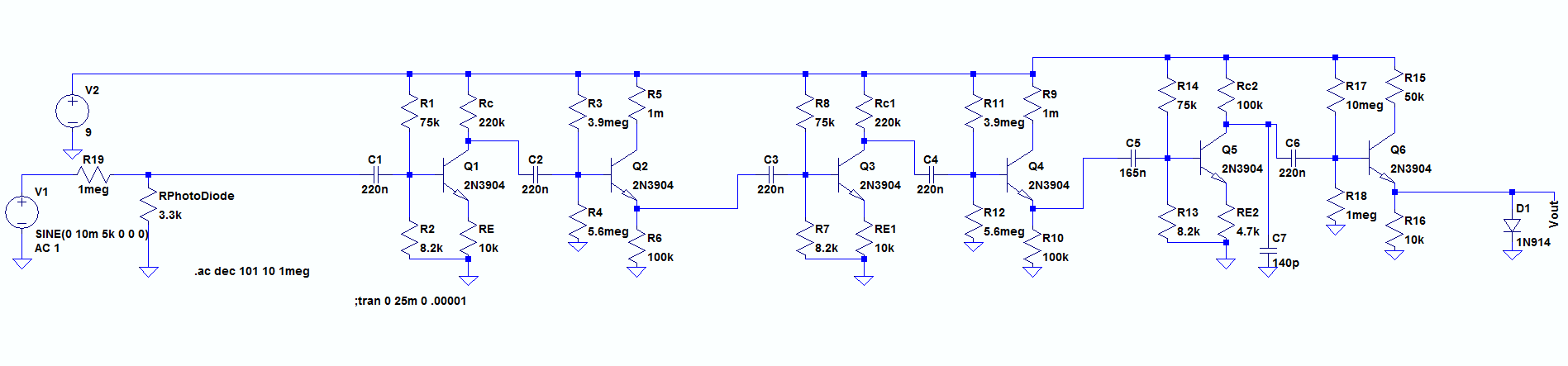


Figure 13 final LTSpice schematic

After building the circuit on the breadboard, we began testing. We first tried to measure the gain across the first two stages. The output voltage (figure 2) divided by the input voltage (figure 3) equaled 280.5.



Figure 14 output voltage across two stages

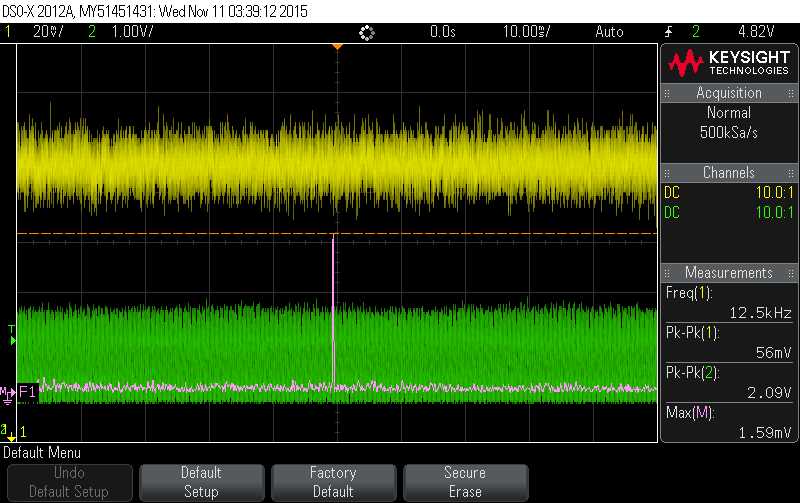


Figure 15 input voltage across two stages

We then tried to measure the gain across all three stages. The output (figure 4) divided by the input (figure 5) equaled 280. This was definitely well below the gain that we were aiming for. However, we can see from the output voltage that there is a considerable amount of clipping going on.

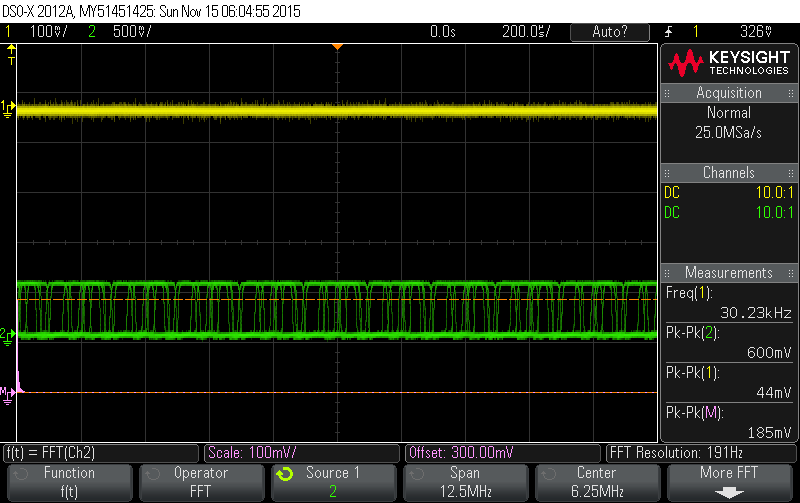


Figure 16 output voltage across three stages without diode

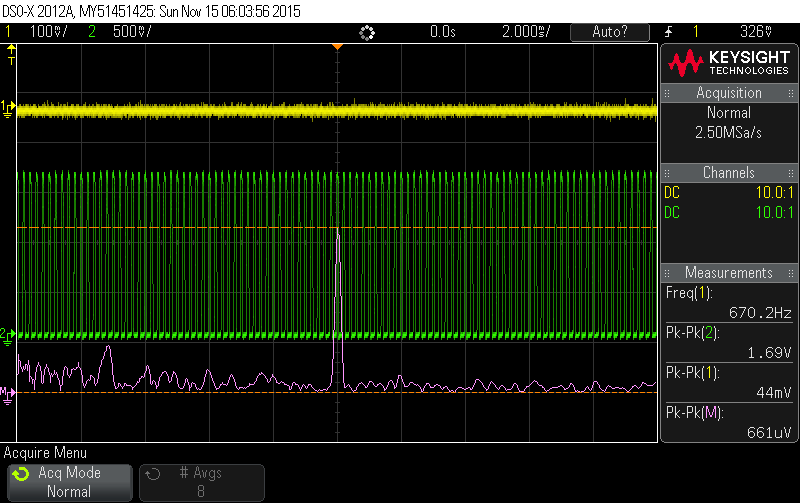


Figure 17 input voltage across three stages

We saw that there was basically no gain across the third stage. After closer inspection and some calculations, we noticed that the final CE BJT was in saturation. We had to change the 120kΩ on the final CE stage to a 100kΩ resistor, because the LTSpice simulation had not taken into account the state of the BJT. Because of the change on that resistor we had to recalculate the capacitor value needed to achieve the upper corner frequency as well.

With the redesigned circuit we again measured the gain at 2 kHz, which should have no attenuation. The output voltage (figure 6) divided by the input voltage (figure 7) equaled 8.63. We had the MΩ resistor at the beginning of the circuit, so this would be equivalent to 8.63 million V/A gain, which meets the specs.



Figure 18 output voltage @ 2 kHz

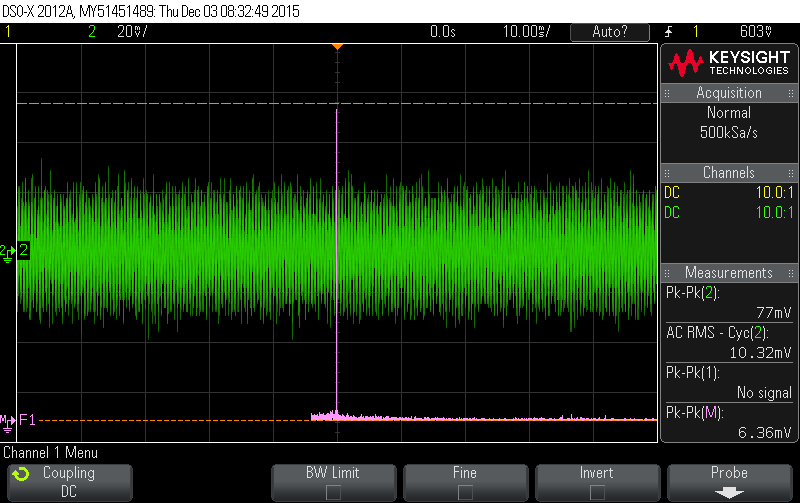


Figure 19 input voltage @ 2kHz

Using the oscilloscope we were able to determine our lower corner frequency to be 280 Hz (figure 8) and our upper corner frequency to be 10.9 kHz (figure 9). These were relatively close to our calculations that yield a lower frequency of 170 Hz and an upper frequency of 10.9 kHz.

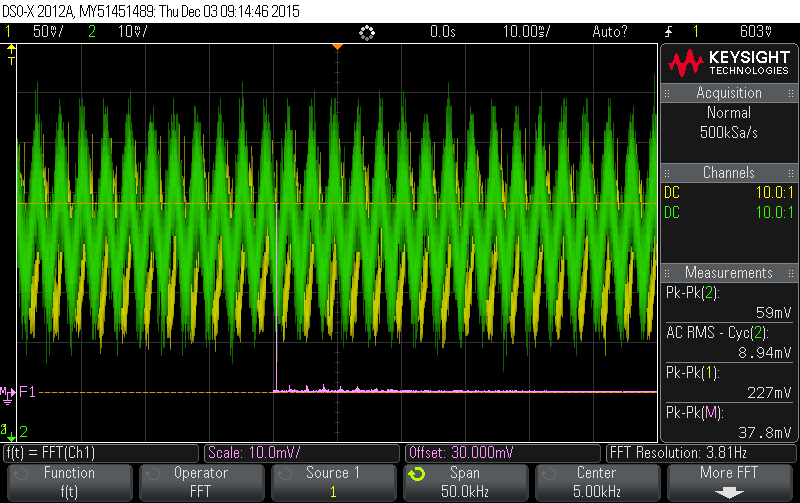


Figure 20 lower corner frequency - 280 Hz



Figure 21 upper corner frequency - 10.9 kHz

After the tests on our corner frequencies, we measured our power consumption. Within a reasonable input voltage we saw that the maximum power consumption from the battery is around 0.66 mA.

-Simulations for gain

-Calculations for capacitors and bandpass filtering

-Simulations of frequency response

-Calculations for output impedance and diode

-Simulations of power consumption and saturation behavior

-Put final schematic

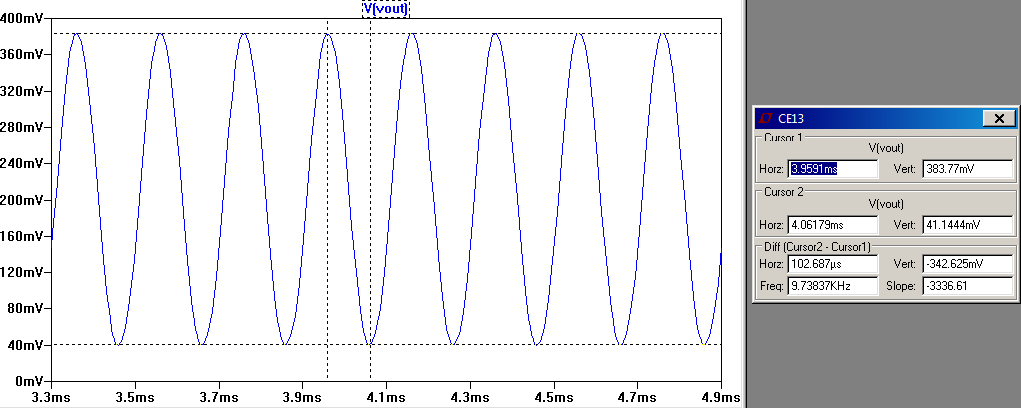
-Talk about breadboarding. We built stages at a time

-Talk about 3rd CE stage saturation

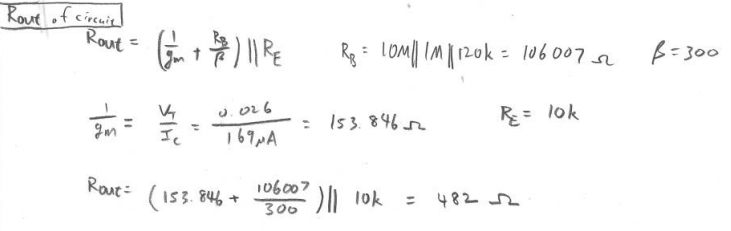
Gain calculations:

Gain simulation:

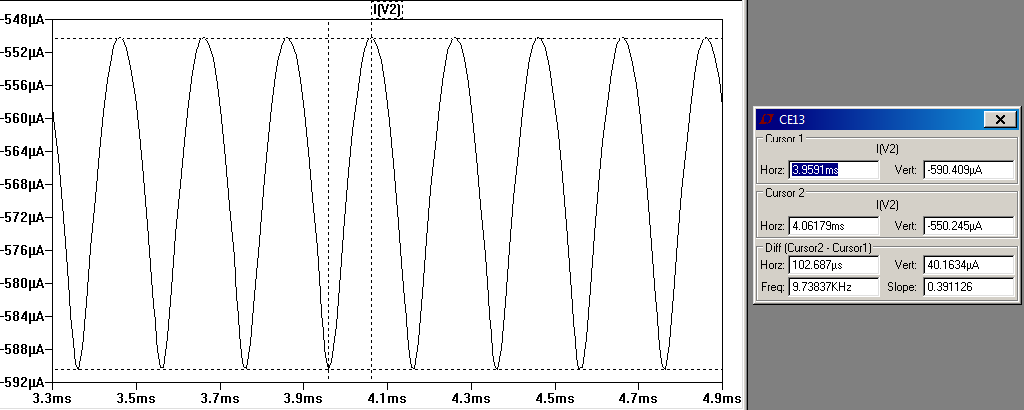
20 n



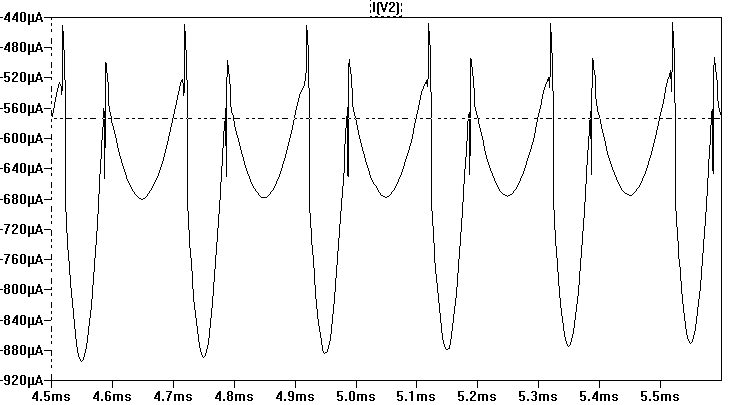
Output impedance calculations



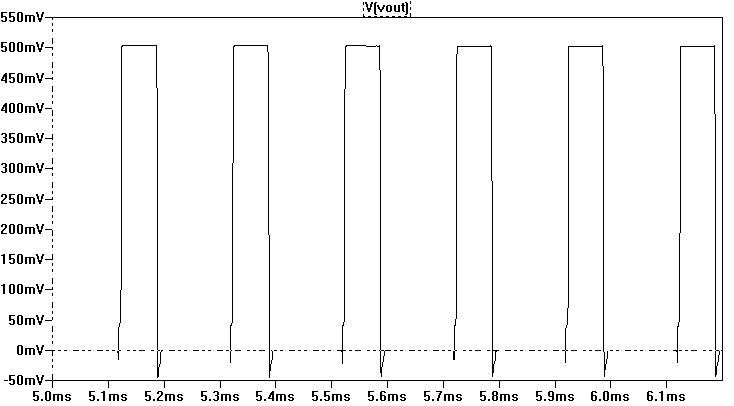
Power consumption 20nA



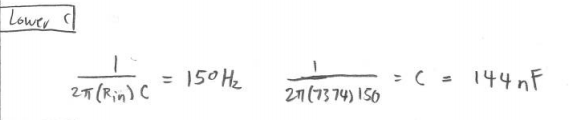
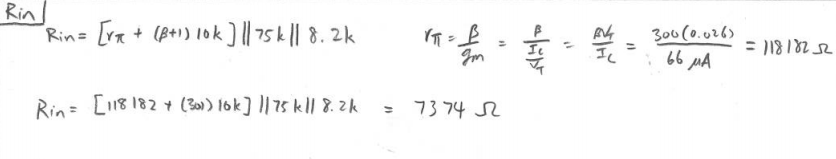
Power consumption 100uA



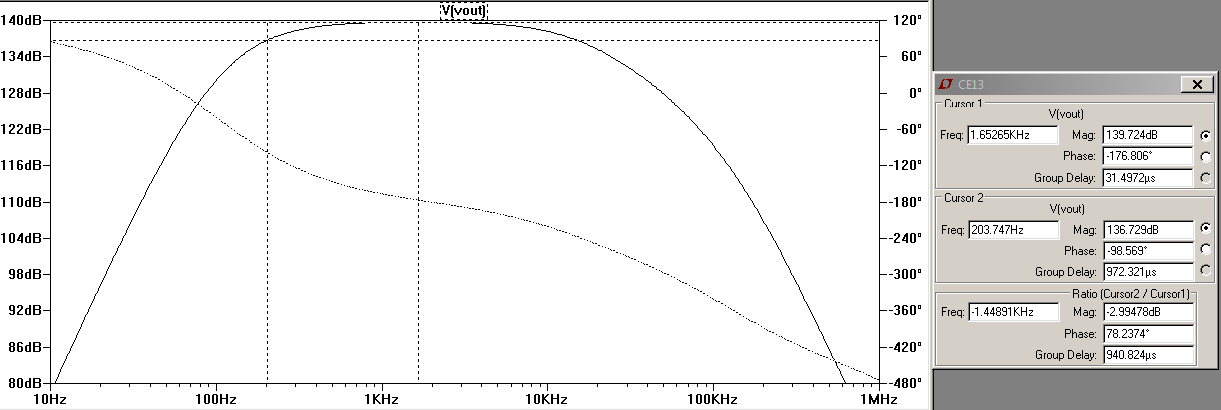
Output limiting at 100uA



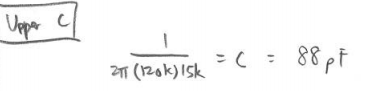
Lower corner frequency calculations



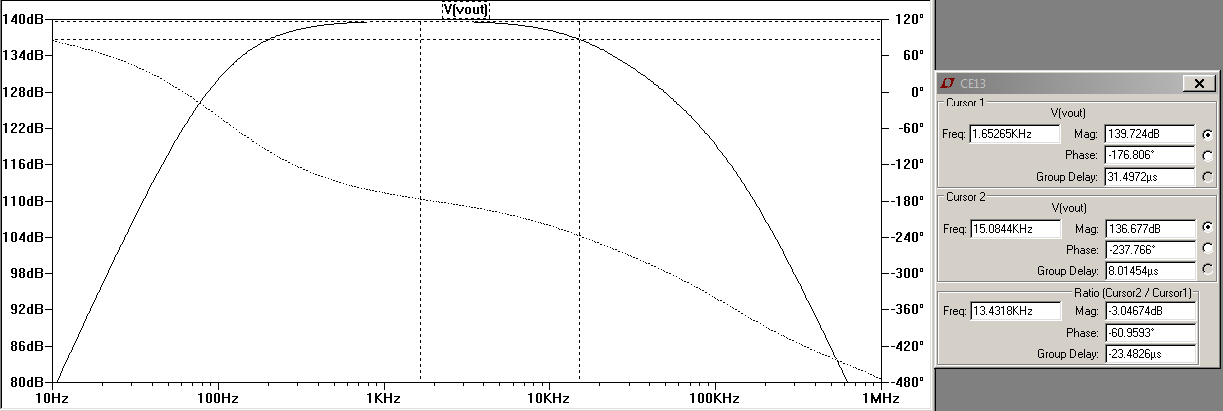
Frequency response lower corner at 20nA



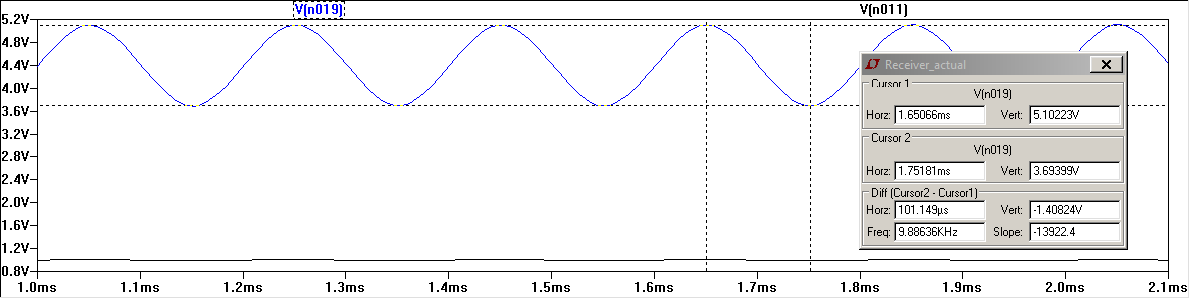
Upper corner frequency calculations



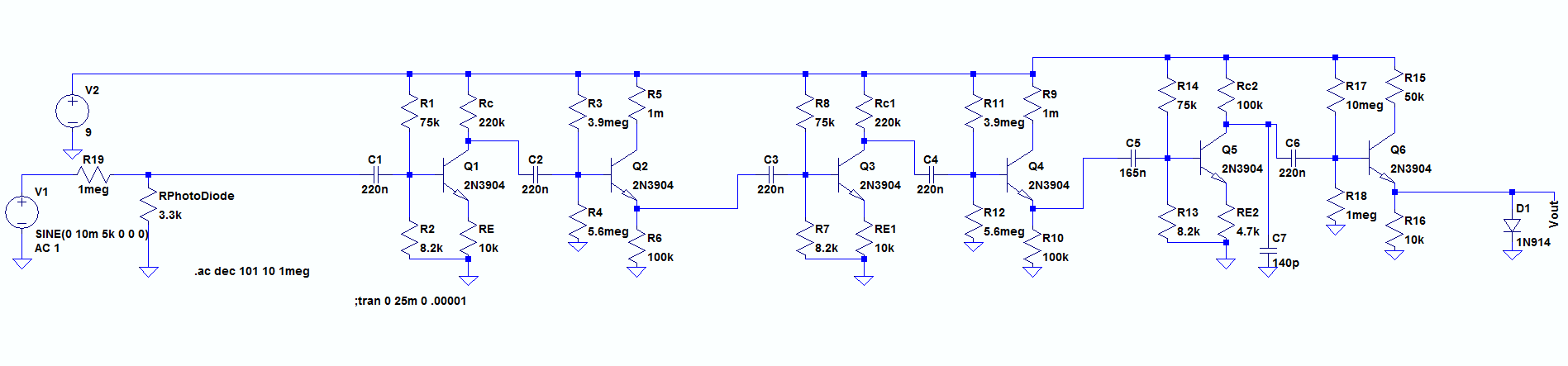
Frequency response upper corner at 20nA



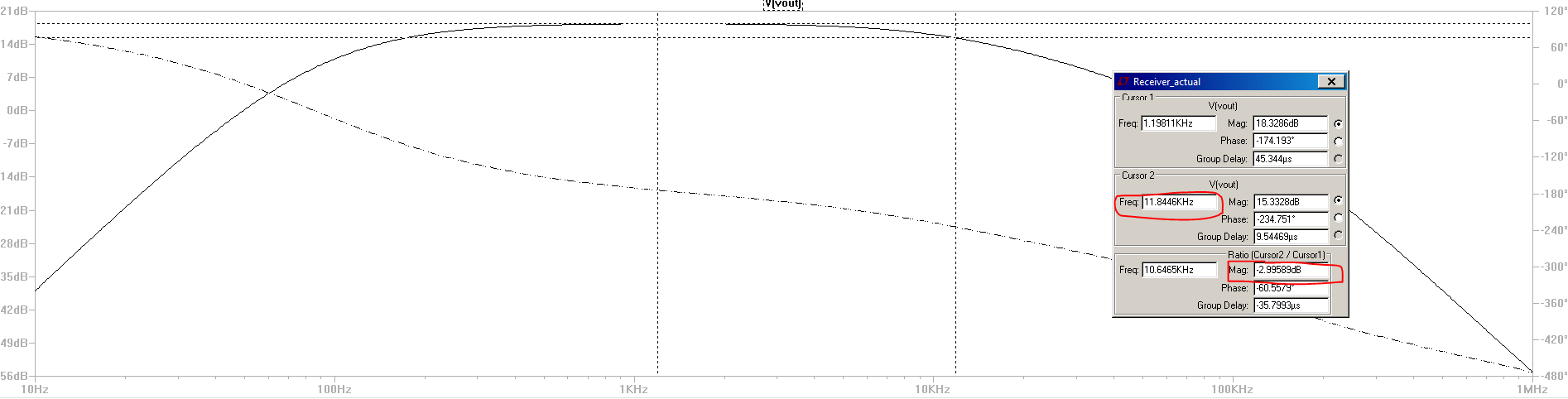
Testing 2 stages



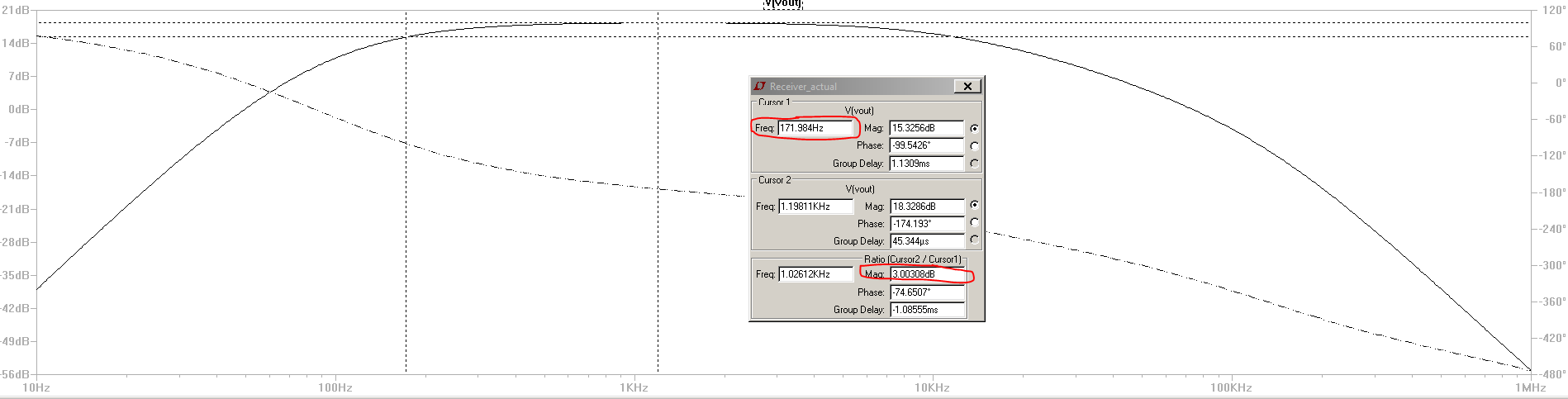
Final Schematic



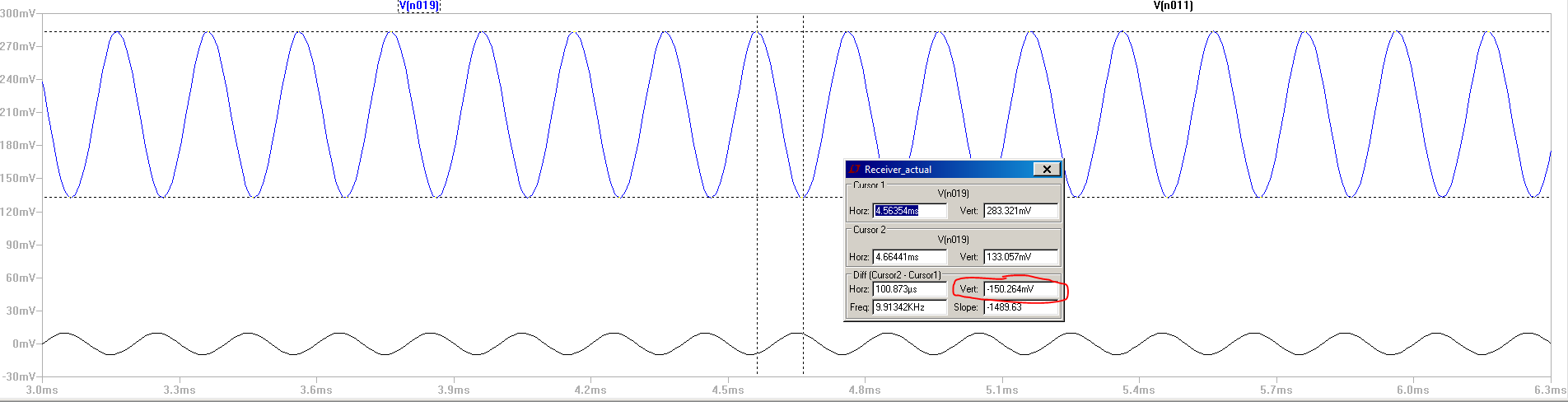
Final Upper corner freq



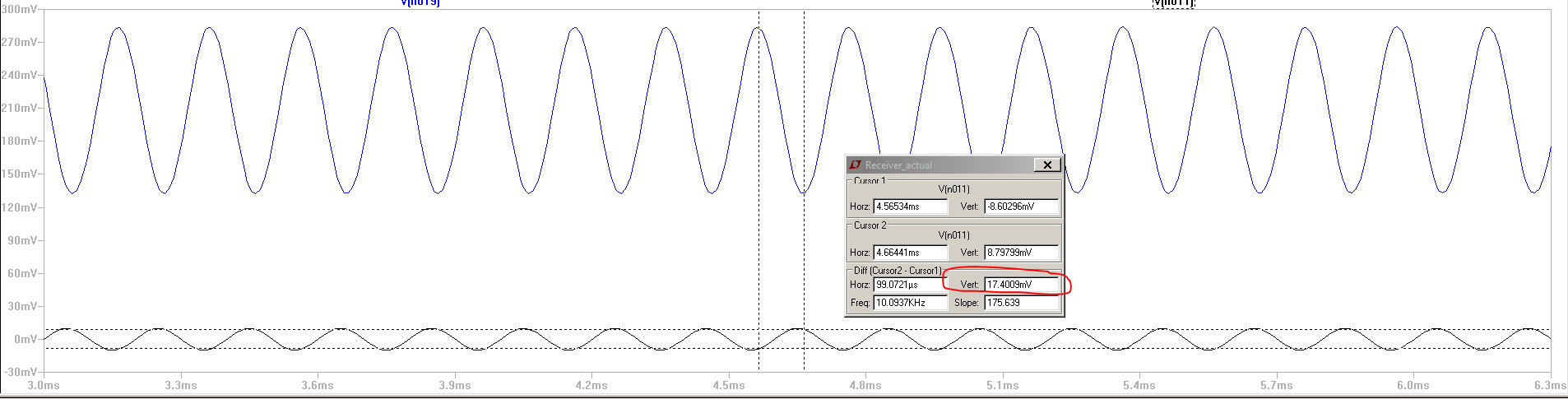
Final lower corner freq



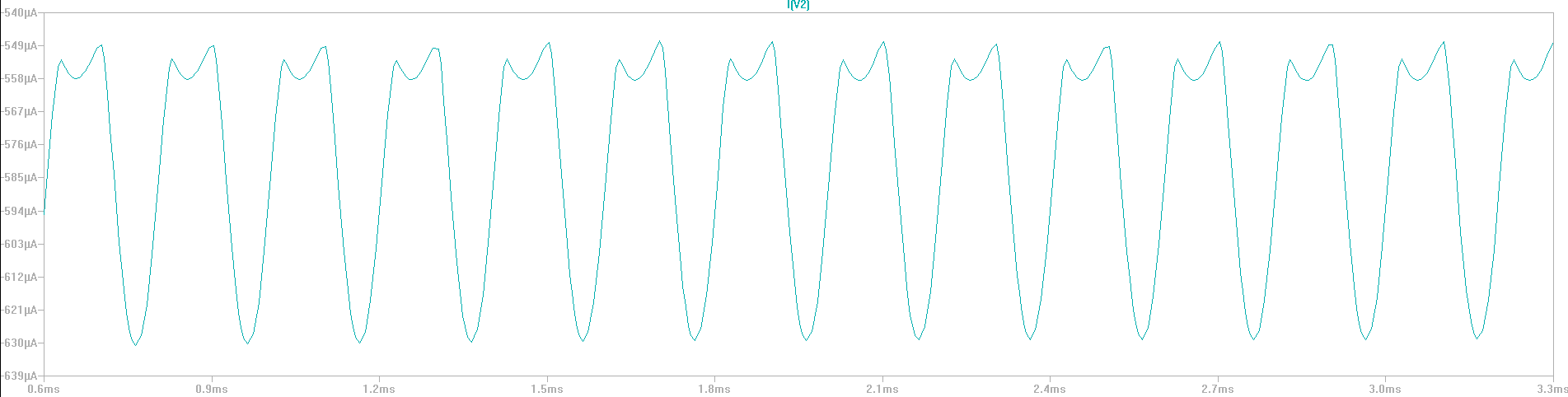
Final gain – output



Final gain input



Final current draw



Conclusion

In this lab, we designed a circuit to amplify a signal from a photodiode so that it can be used by the Zybo board. This entailed not only amplifying the signal, but also limiting the output voltage and bandwidth as well as ensuring that the entire system does not consume too much power. Working to meet these requirements not only helped us apply our knowledge about BJT circuit topologies, but also gave us practical experience with issues related to amplifier circuits.

The final circuit was broken down into three major parts for us by the lab instructions: the photodiode/resistance combination, the voltage amplification stage, and the voltage limiter. The design of the first of these three was already given to us, so it was up to us to design the latter two.

The voltage amplification stage was the first part that we designed and was the more difficult of the two.